

EXAM II ANSWERS

1) The first two analysis steps are completed and the following equations are given :

$$\overrightarrow{y_2} = \overline{x} \overline{y_2} \overline{y_1} + \overline{x} y_2 y_1 + x y_2 \overline{y_1} + x \overline{y_2} y_1$$

$$\overrightarrow{y_1} = \overline{y_1} \qquad \overrightarrow{y_0} = y_0$$

$z_2 = y_2 \qquad z_1 = y_1 \qquad z_0 = y_0$

This is a **Moore** circuit : The sequential circuit outputs z2, z1 and z0 are independent of x. That is, the z2, z1 and z0 equations do not contain "x" as one of the variables. The analysis of the sequential circuit is continued :

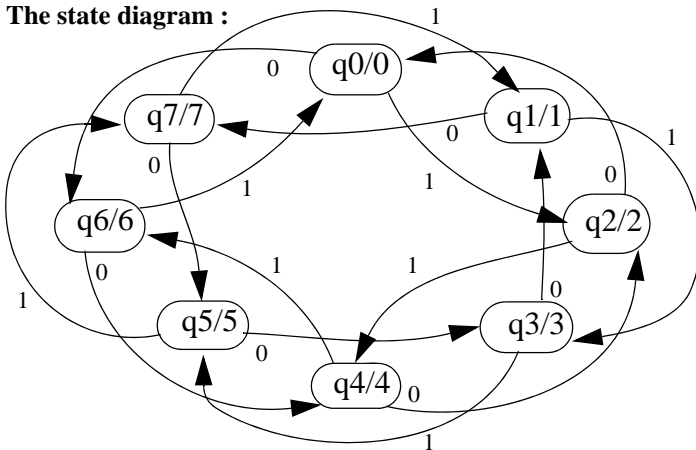
c) The excitation table :

	$y_2 y_1 y_0$	$\overrightarrow{y_2} \overrightarrow{y_1} \overrightarrow{y_0}$		$z_2 z_1 z_0$	
		$x=0$	$x=1$	$x=0$	$x=1$
		q0	000	1 1 0	0 1 0
q1	001	1 1 1	0 1 1	001	001
q2	010	0 0 0	1 0 0	010	010
q3	011	0 0 1	1 0 1	011	011
q4	100	0 1 0	1 1 0	100	100
q5	101	0 1 1	1 1 1	101	101
q6	110	1 0 0	0 0 0	110	110
q7	111	1 0 1	0 0 1	111	1111

d) The state table :

PS	NS		OUT
	x=0	x=1	
q0	q6	q2	0
q1	q7	q3	1
q2	q0	q4	2
q3	q1	q5	3
q4	q2	q6	4
q5	q3	q7	5
q6	q4	q0	6
q7	q5	q1	7

e) The state diagram :



f) The functional description :

(i) Timing analysis :

Time	t0	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11...
x	0	0	0	0	0	0	1	1	1	1	1	1...
PS	q3	q1	q7	q5	q3	q1	q7	q1	q3	q5	q7	q1...
OUT	3	1	7	5	3	1	7	1	3	5	7	1...

Time	t0	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11...
x	1	1	1	1	1	1	0	0	0	0	0	0...
PS	q6	q0	q2	q4	q6	q0	q6	q4	q2	q0	q6	q4...
OUT	6	0	2	4	6	0	6	4	2	0	6	4...

(ii) Purpose : This is a 3-bit up/down counter. When input "x" is 0, it counts down by 2. When input "x" is 1, it counts up by 2

2) The table is continued below :

T	Shift	x	a b c d	Gt	Store	z3 z2 z1 z0	Valid
t0	0	0	0 0 0 0	0	0	0 0 0 0	1
t1	1	0	0 0 0 0	0	0	0 0 0 0	0
t2	1	1	0 0 0 0	0	0	0 0 0 0	0
t3	1	0	0 0 0 1	1	0	0 0 0 0	0
t4	1	1	0 0 1 0	1	0	0 0 0 0	0
t5	0	0	0 1 0 1	1	1	0 0 0 0	1
t6	1	1	0 1 0 1	0	0	0 1 0 1	0
t7	1	0	1 0 1 1	1	0	0 1 0 1	0
t8	1	0	0 1 1 0	1	0	0 1 0 1	0
t9	1	1	1 1 0 0	1	0	0 1 0 1	0
t10	0	0	1 0 0 1	1	1	0 1 0 1	1
t11	1	1	1 0 0 1	0	0	1 0 0 1	0
t12	1	1	0 0 1 1	0	0	1 0 0 1	0
t13	1	1	0 1 1 1	0	0	1 0 0 1	0
t14	1	0	1 1 1 1	1	0	1 0 0 1	0
t15	0	0	1 1 1 0	1	1	1 0 0 1	1
t16	1	1	1 1 1 0	0	0	1 1 1 0	0

The sequential circuit accepts 4-bit numbers serially on input “x”.

It compares these 4-bit input numbers, “a b c d” with the current largest number, “z3 z2 z1 z0”. If the current 4-bit number is larger than current largest number, it stores it as the current largest.

The numbers compared are Unsigned Binary numbers.

The “Valid” output indicates that a 4-bit number has been obtained from the serial input and a compare has just been done and the “z3 z2 z1 z0” outputs may have a new current largest value the following clock period.

One has to read the “z3 z2 z1 z0” output one clock period after the “Valid” output is 1 for proper timing.

The sequential circuit does these continuously.

3) The table is completed below. The displays played on are shown in bold and circled :

RD	Displays Before Play PD3 PD2 PD1 PD0				Displays After Play PD3 PD2 PD1 PD0				D/A	The Adjacency	Points Earned (Decimal)	Machine player plays again
2	E	6	E	6	E	6	E	8	A	0	72	N
5	5	5	A	A	5	5	5	A	D	2	20	Y
8	7	7	7	7	7	7	7	F	A	0	15	N
0	F	E	F	F	F	E	F	F	A	1	30	Y
4	6	A	B	A	A	A	B	A	A	1	20	Y

We observe that the machine player misses a chance to earn code reward points when RD is 5, 8, 0 and 4. However, by chance, it earns code reward points when RD is 2.