

HOMEWORK III

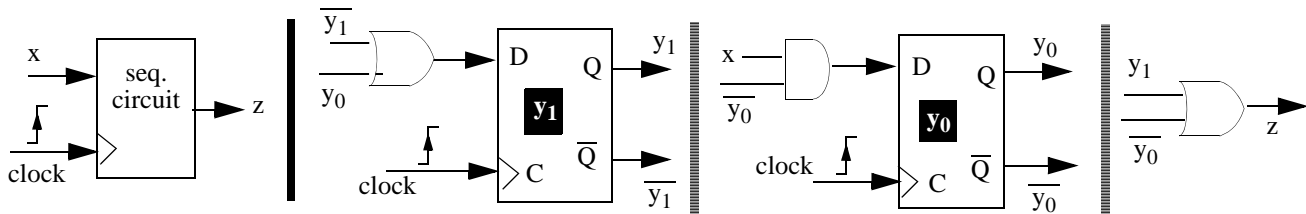
DUE : October 27, 2011

READ : Related portions of Chapters VII and VIII

ASSIGNMENT : There are three questions.

Solve all homework and exam problems as shown in class and past exam solutions.

1) Consider the following sequential circuit :

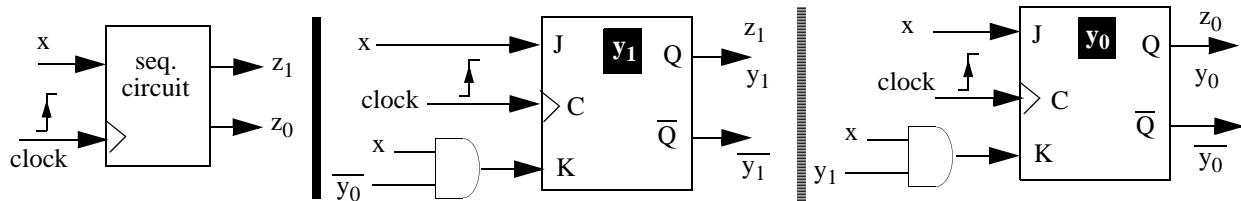


Analyze the sequential circuit in the style shown in class. This question is identical to textbook problem 7.12 except that FF y_2 is renamed y_0 .

Note that this circuit does not seem to have a purpose. Nevertheless, do a timing analysis and write that there is no purpose.

Note also that this is a Moore circuit since the only sequential circuit output, z , is not a function of input x . Also, this is a **non-finite memory** circuit since the FFs do not form a shift register.

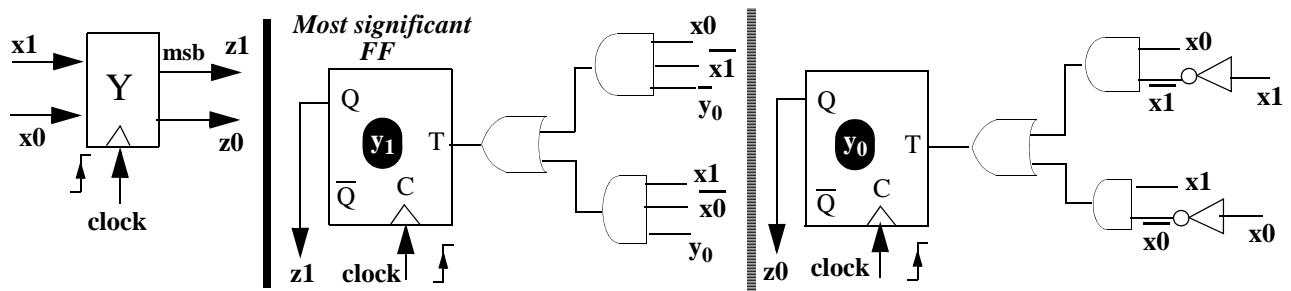
2) Consider the following sequential circuit :



Analyze the sequential circuit in the style shown in class.

Since FF y_1 output is sequential circuit output z_1 and FF y_0 output is sequential circuit output z_0 , this circuit is also a Moore circuit : The sequential circuit outputs, z_1 and z_0 , are not a function of input x . Finally, this is a **non-finite memory** circuit since the FFs do not form a shift register.

3) Consider the following sequential circuit :

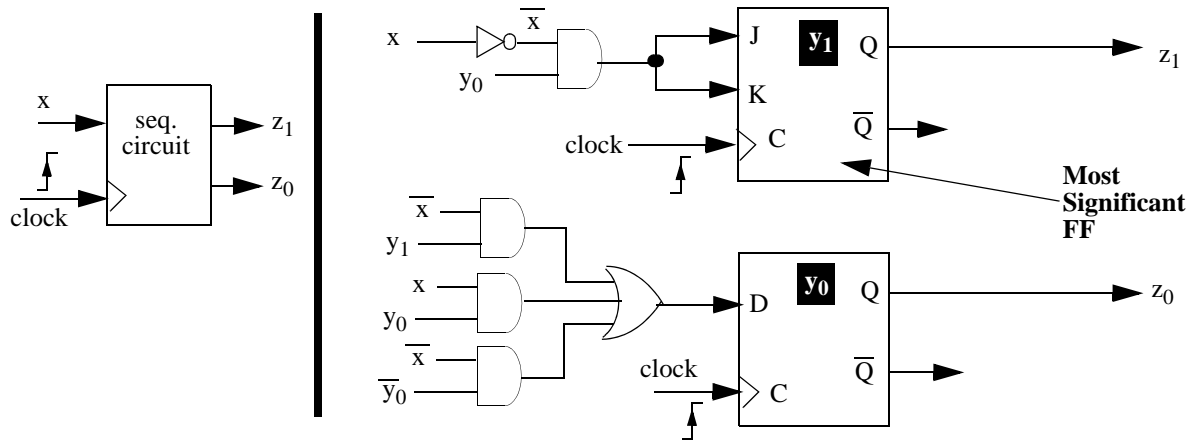


Analyze the sequential circuit in the style shown in class.

Note that there are 2 (two) inputs hence there are four sets of next state columns. Is this sequential circuit a Moore or Mealy circuit ? Why ?

RELEVANT QUESTIONS AND ANSWERS

Q1) Consider the following **sequential** circuit :



Analyze the sequential circuit in the style shown in class. Is this circuit a Mealy or Moore circuit ? Why ?

FF y_1 is the most significant FF. The FF y_1 output is sequential circuit output z_1 and the FF y_0 output is sequential circuit output z_0 .

A1) a) Flip-flop input and sequential circuit output equations :

$$J_1 = \bar{x} y_0$$

$$D_0 = \bar{x} y_1 + x y_0 + \bar{x} \bar{y}_0$$

$$z_1 = y_1$$

$$K_1 = \bar{x} y_0$$

$$z_0 = y_0$$

Since sequential circuit outputs z_1 and z_0 do not depend on x , this is a Moore circuit.

b) Next flip-flop output (next state) equations :

$$\begin{aligned} \vec{y}_1 &= J_1 \bar{y}_1 + \bar{K}_1 y_1 = (\bar{x} y_0) \bar{y}_1 + (\bar{x} \bar{y}_0) y_1 \\ &= \bar{x} \bar{y}_1 y_0 + [(\bar{x} + \bar{y}_0)] y_1 \\ &= \bar{x} \bar{y}_1 y_0 + x y_1 + y_1 \bar{y}_0 \end{aligned} \quad \left| \quad \vec{y}_0 = D_0 = \bar{x} y_1 + x y_0 + \bar{x} \bar{y}_0 \right.$$

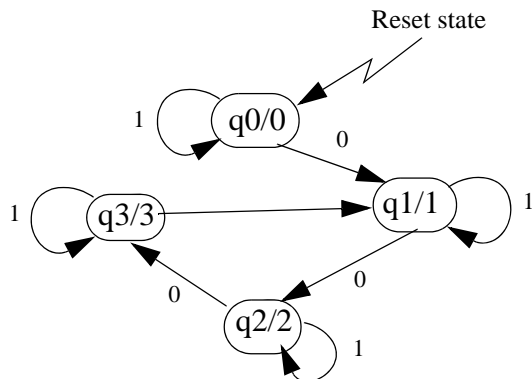
c) The excitation table :

$y_1 y_0$	\vec{y}_1		\vec{y}_0	
	$x=0$	$x=1$	$x=0$	$x=1$
00	01	00	00	00
01	10	01	01	01
10	11	10	10	10
11	01	11	11	11

d) The state table :

PS	NS		OUT
	$x=0$	$x=1$	
q0	q1	q0	0
q1	q2	q1	1
q2	q3	q2	2
q3	q1	q3	3

e) The state diagram :



f) The functional description :

(i) Timing analysis :

Time	t0	t1	t2	t3	t4	t5	t6	t7	t8 ...
x	1	0	0	0	1	0	0	0	0 ...
PS	q0	q0	q1	q2	q3	q3	q1	q2	q3 ...
OUT	0	0	1	2	3	3	1	2	3 ...

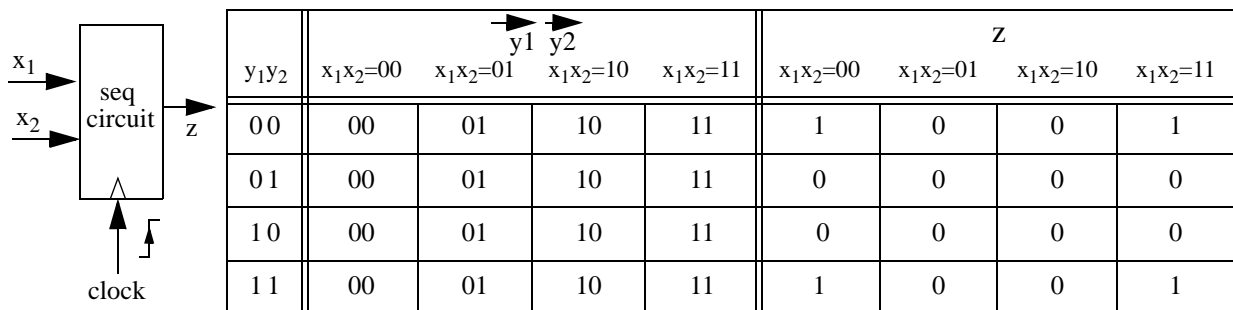
(ii) The Purpose :

It is a **2-bit binary** (modulo-3, divide-by-3) **up counter**.
It starts with zero and then counts as 1, 2, 3, 1,...

It counts up by one when x is 0 : 0, 1, 2, 3, 1, 2, 3,...

The count does **not** change when x is 1.

Q2) Consider the sequential circuit below with two inputs and one output. Its transition table (excitation table) is also given. Continue the analysis. The labeling of FFs is the opposite of our convention, but, we will keep it :

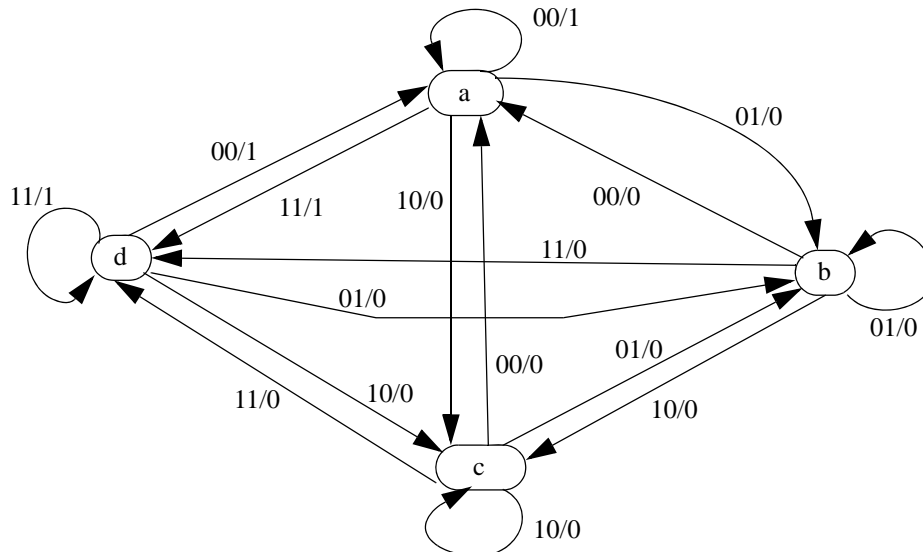


A2) Note that the transition table indicates that this is a **Mealy** circuit, since output (z) columns are not identical, i.e. the output z depends on the values of inputs x_1 and x_2 . Also, this is a **finite-input memory** circuit where the inputs one clock period earlier are remembered.

d) The state table is obtained directly from the excitation table :

y_1y_2	NS				OUT			
	$x_1x_2=00$	$x_1x_2=01$	$x_1x_2=10$	$x_1x_2=11$	$x_1x_2=00$	$x_1x_2=01$	$x_1x_2=10$	$x_1x_2=11$
a	a	b	c	d	1	0	0	1
b	a	b	c	d	0	0	0	0
c	a	b	c	d	0	0	0	0
d	a	b	c	d	1	0	0	1

e) The state diagram :



f) The functional description :

(i) Timing analysis : assume that the following arbitrary input sequence is given to the sequential circuit :

Assume also that the initial state is "a." Then :

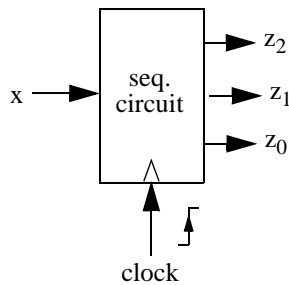
x_1x_2 → 10 00 11 01 10 11 00 00 → time

Time	t0	t1	t2	t3	t4	t5	t6	t7.....
x_1x_2	10	00	11	01	10	11	00	00.....
PS	a	c	a	d	b	c	d	a.....
OUT	0	0	1	0	0	0	1	1.....

(ii) The purpose : the circuit outputs a 1, if for two successive clock periods $x_1=x_2$. The output is 1 for one clock period when it detects that the inputs are equal to each other the second time. For example, above $x_1=x_2=0$ at t1 and $x_1=x_2=1$ at t2. Two consecutive clock periods they are equal to each other, thus output z is raised to 1 at t2, for one

clock period. **Overlapping** of successive checkings is allowed. For example, at t5, t6 and t7 the inputs are equal to each other, thus, the output is 1 at t6 since $x_1=x_2$ at t5 and t6 and again 1 at t7, as $x_1=x_2$ at t6 and t7.

Q3) Determine the purpose of the following sequential circuit which has one input and three outputs. Its excitation table is also shown below :



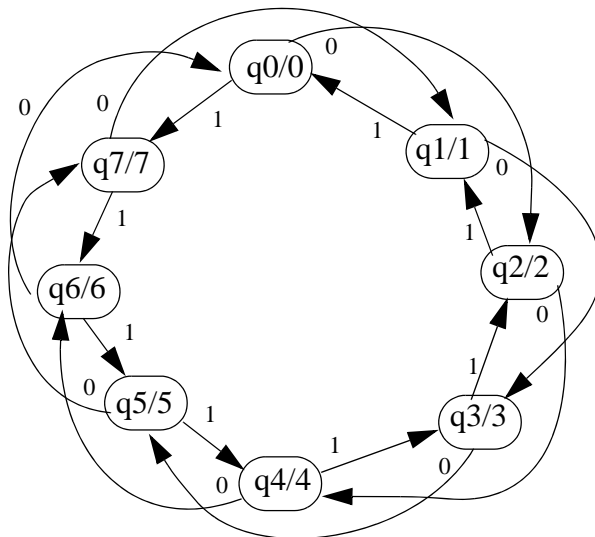
d	e	f	x		z ₂ z ₁ z ₀	
			x = 0	x = 1	x = 0	x = 1
0	0	0	0	1	0	0
0	0	1	0	1	0	0
0	1	0	1	0	0	1
0	1	1	1	0	1	1
1	0	0	1	1	0	0
1	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	1	0	0	1	1

A3) The analysis of the sequential circuit in the question continues : first we obtain the state table, then state diagram and finally, the timing analysis is done.

The state table :

PS	NS		OUT	
	x=0	x=1	x=0	x=1
q0	q2	q7	0	0
q1	q3	q0	1	1
q2	q4	q1	2	2
q3	q5	q2	3	3
q4	q6	q3	4	4
q5	q7	q4	5	5
q6	q0	q5	6	6
q7	q1	q6	7	7

The state diagram :



We observe that the output is **independent** of the input, which indicates that this is a **Moore** circuit.

Functional Description :

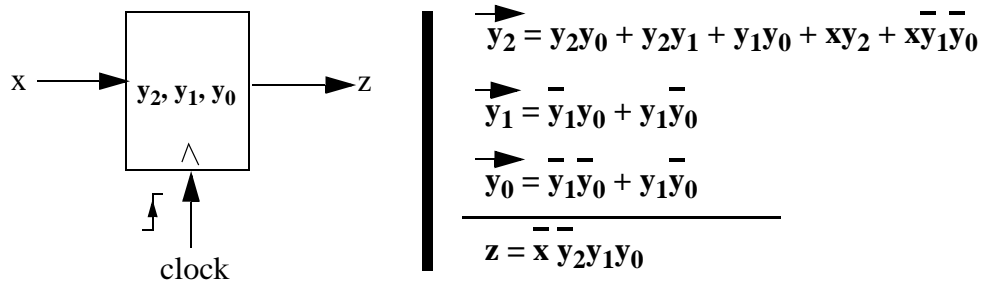
The timing analysis :

time	t0	t1	t2	t3	t4	t5	t6	t7	t8 ...
x	1	1	1	0	0	0	0	1	1 ...
PS	q0	q7	q6	q5	q7	q1	q3	q5	q4 ...
OUT	0	7	6	5	7	1	3	5	4

Purpose :

We realize that this is a modulo-8 counter that when the input is 1, the sequential circuit counts **down by 1** and when the input is 0, it **counts up by 2**.

Q4) A sequential circuit has three flip-flops, named y_2 , y_1 and y_0 . The black box view, flip-flop output equations (next state equations) and the sequential circuit output equation are shown below:



Continue the analysis of the sequential circuit as shown in class to determine its purpose. Note that flip-flop y_2 is the most significant flip-flop. Is this sequential circuit a Moore or Mealy circuit? Why? Explain in a single sentence.

A4) We continue with the analysis :

c) The excitation table :

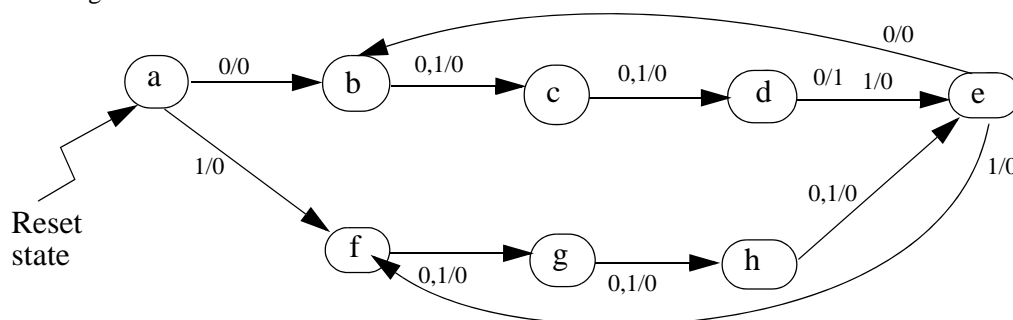
$y_2 y_1 y_0$	$\vec{y}_2 \vec{y}_1 \vec{y}_0$		z	
	$x=0$	$x=1$	$x=0$	$x=1$
000	001	101	0	0
001	010	010	0	0
010	011	011	0	0
011	100	100	1	0
100	001	101	0	0
101	110	110	0	0
110	111	111	0	0
111	100	100	0	0

d) The state table :

PS	NS		OUT	
	$x=0$	$x=1$	$x=0$	$x=1$
a	b	f	0	0
b	c	c	0	0
c	d	d	0	0
d	e	e	1	0
e	b	f	0	0
f	g	g	0	0
g	h	h	0	0
h	e	e	0	0

It is a **Mealy** circuit since the sequential circuit output z **depends** on input x . Also, it is a **non-finite memory** circuit since the state table is not the standard state table for three FFs.

e) The state diagram :

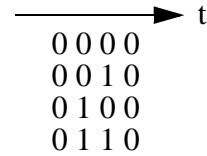


f) The purpose of the circuit :

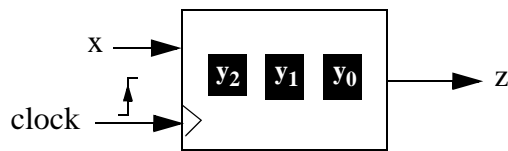
(i) Timing analysis :

time	t0	t1	t2	t3	t4	t5	t6	t7	t8
x	0	1	0	0	0	0	0	1	1
PS	a	b	c	d	e	b	c	d	e
OUT	0	0	0	1	0	0	0	0	0

(ii) The Purpose : it recognizes 4-bit distinct **nonoverlapping** sequences shown below and outputs a 1 for one clock period, when it receives the last bit of the correct sequence :



Q5) Consider the following 1-input, 1-output **sequential** circuit with **three** flip-flops :



FF y_2 is the most significant FF. The first **two** analysis steps are already completed. The following are the sequential circuit **output** equation and next flip-flop output (**next state**) equations :

$$\vec{y}_2 = x \quad \vec{y}_1 = y_2 \quad \vec{y}_0 = y_1 \quad z = \bar{x} y_2 y_1 \bar{y}_0$$

Continue the analysis of the sequential circuit as shown **in class**. Is this circuit a **Mealy** or **Moore** circuit ? Explain why. Is this a **non-finite** memory or **finite** memory circuit ? Explain why.

A5) The analysis steps continue with the excitation table and state table steps below :

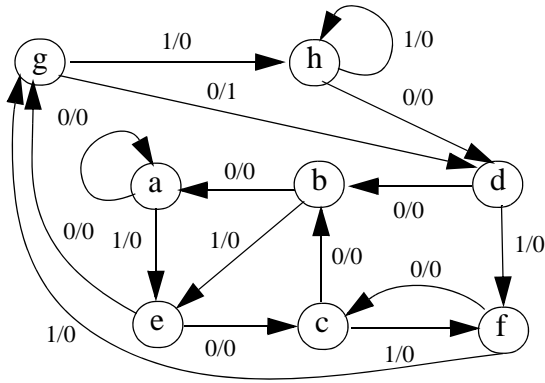
c) The excitation table :

	$y_2 y_1 y_0$	$\vec{y}_2 \vec{y}_1 \vec{y}_0$		z	
		x=0	x=1	x=0	x=1
a	000	000	100	0	0
b	001	000	100	0	0
c	010	001	101	0	0
d	011	001	101	0	0
e	100	010	110	0	0
f	101	010	110	0	0
g	110	011	111	1	0
h	111	011	111	0	0

d) The state table :

PS	NS		OUT	
	x=0	x=1	x=0	x=1
a	a	e	0	0
b	a	e	0	0
c	b	f	0	0
d	b	f	0	0
e	c	g	0	0
f	c	g	0	0
g	d	h	1	0
h	d	h	0	0

e) The state diagram :



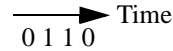
f) The functional description :

(i) Timing analysis :

Time	t0	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11	t12...
x	0	1	1	0	1	1	0	1	1	1	0	1	1...
PS	a	a	e	g	d	f	g	d	f	g	d	f	g...
OUT	0	0	0	1	0	0	1	0	0	0	0	0	0...

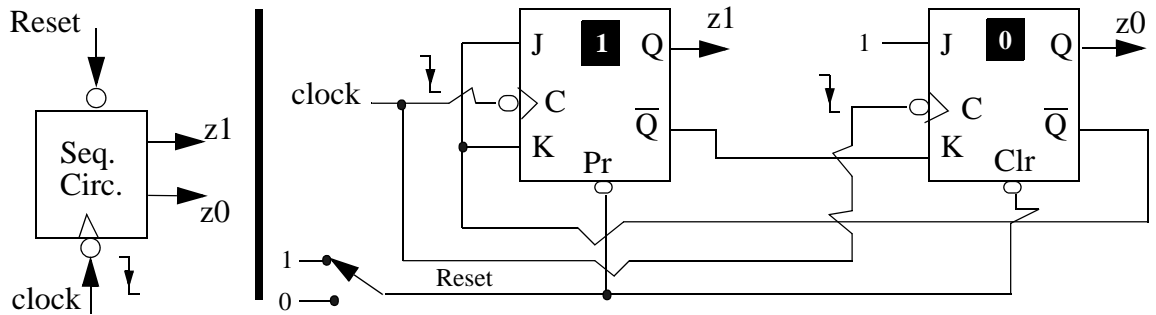
(ii) The Purpose :

It is a sequence detector that checks for every overlapping sequence that has a 0 then 1 then a 1 and then a 0. It outputs a 1 for one clock period when it receives the last bit of the correct sequence. It never stop checking :



This is a **Mealy** circuit : The sequential circuit output depends on input x. This a **finite** memory sequential circuit : It remembers the last three inputs which can be deduced from the state table : The standart state table for three FFs.

Q6) Analyze the following sequential circuit as shown in class :



A6) This is an unusual circuit, but, such circuits are used in real life. The circuit does not really have an input in the sense we are used to. Because, the Reset input is connected to the Direct Preset and Direct Clear inputs, not to the J and K inputs. The Reset input places the sequential circuit in a “reset state” when it is active (in this example, it is active-low) and keeps it there as long as it is active. Once, it becomes inactive (i.e. 1), the circuit is “on its own.”

Therefore, our analysis will apply only **when the Reset input is inactive, 1**. When Reset is 0, we see that FF1 is 1 and FF0 is 0. Thus, the reset state is “10” and the sequential circuit stays at “10” as long as the Reset input is 0. When the Reset input is 1, then FFs can have other values, thus the state of the sequential circuit can change.

a) FF input equations and sequential circuit output equations (when the Reset input is inactive, 1) :

$$\begin{aligned}
 J_1 &= \overline{Q_0} & J_0 &= 1 \\
 K_1 &= \overline{Q_0} & K_0 &= \overline{Q_1} \\
 z1 &= Q1 & z0 &= Q0
 \end{aligned}$$

b) Next state equations (when the Reset input is inactive, 1) :

$$\begin{aligned}
 \overrightarrow{Q_1} &= J_1 \overline{Q_1} + \overline{K_1} Q_1 = \overline{Q_0} \overline{Q_1} + \overline{\overline{Q_0}} Q_1 = \overline{Q_0} \overline{Q_1} + Q_0 Q_1 \\
 \overrightarrow{Q_0} &= J_0 \overline{Q_0} + \overline{K_0} Q_0 = 1 \overline{Q_0} + \overline{\overline{Q_1}} Q_0 = \overline{Q_0} + Q_1 Q_0 = \overline{Q_0} + Q_1
 \end{aligned}$$

The sequential circuit outputs are connected directly to the outputs of the FF's. That is, the outputs are a function of the current state. This is a **Moore** circuit....

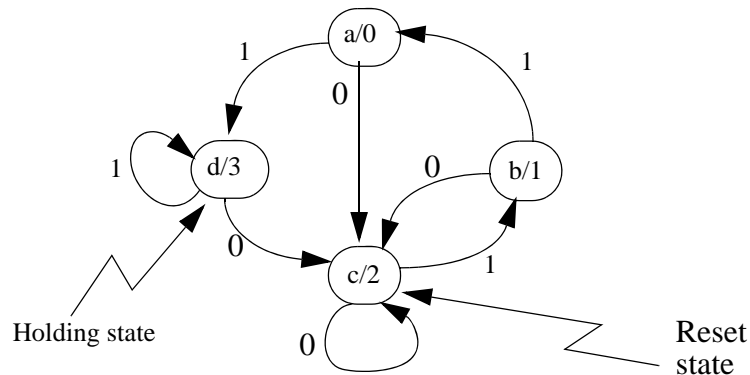
c) The state transition table :

Q1Q0	→ →		z1z0
	Q1 Reset = 0	Q0 Reset = 1	
0 0	1 0	1 1	00
0 1	1 0	0 0	01
1 0	1 0	0 1	10
1 1	1 0	1 1	11

d) The state table :

PS	NS		OUT
	Reset = 0	Reset = 1	
a	c	d	0
b	c	a	1
c	c	b	2
d	c	d	3

e) The state diagram :



This is a non-finite memory circuit since it remembers an event that happens long time earlier. Also, the state table is not the standard state table for two FFs.

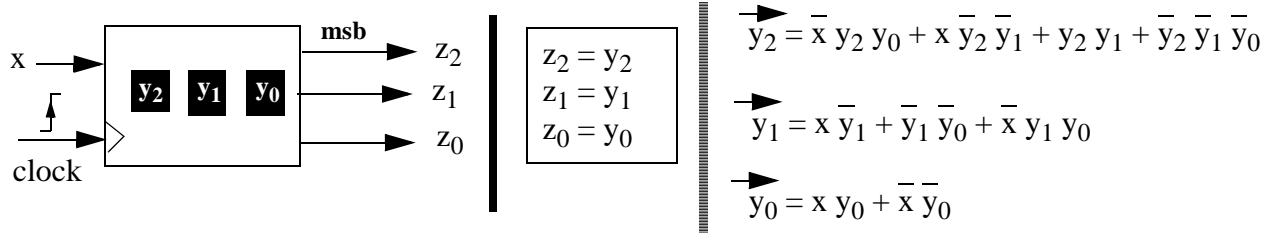
f) The functional description :

(i) timing analysis :

time	t0	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11	t12	t13
Reset	1	1	1	1	1	1	0	1	1	1	1	1	1	1
PS	c	b	a	d	d	d	c	b	a	d	d	d	d	d
OUT	2	1	0	3	3	3	2	1	0	3	3	3	3	3

(ii) The purpose : the circuit is a 2-bit down counter which counts down from 2 to 1 to 0 to 3. After reaching count 3, it stays at that count indefinitely. Therefore, state d is the “holding state.” If the Reset input is activated from any state, the counter immediately returns to the reset state (state c or state 10 or count 2) as the Reset input is an asynchronous input. After Reset goes to 1, the counter reaches count 3 again the same way.

Q7) Consider the 1-input, 3-output **sequential** circuit below with **three** flip-flops. FF **y₂** is the most significant FF. The first **two** analysis steps are already completed. The following are sequential circuit **output** equations and next flip-flip output (**next state**) equations :



Continue the analysis of the sequential circuit as shown in class. Is this circuit a Mealy or Moore circuit? Explain why?

A7) The analysis steps continue with the excitation table and state table steps below :

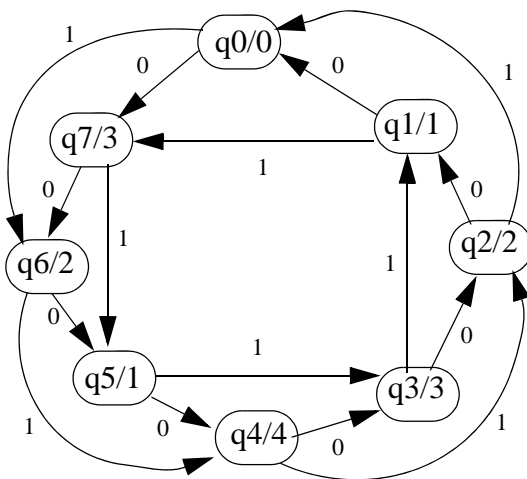
c) The excitation table :

	$y_2 y_1 y_0$	$y_2 y_1 y_0$		$z_2 z_1 z_0$	
		$x=0$	$x=1$	$x=0$	$x=1$
q0	000	111	110	000	000
q1	001	000	111	001	001
q2	010	001	000	010	010
q3	011	010	001	011	011
q4	100	011	010	100	100
q5	101	100	011	101	101
q6	110	101	100	110	110
q7	111	110	101	111	111

d) The state table :

PS	NS		OUT
	$x=0$	$x=1$	
q0	q7	q6	0
q1	q0	q7	1
q2	q1	q0	2
q3	q2	q1	3
q4	q3	q2	4
q5	q4	q3	5
q6	q5	q4	6
q7	q6	q5	7

e) The state diagram :



f) The functional description :

(i) Timing analysis :

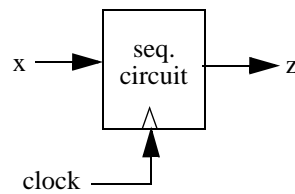
Time	t0	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11	t12...
x	1	1	1	1	1	1	0	0	0	0	0	0	1....
PS	q1	q7	q5	q3	q1	q7	q5	q4	q3	q2	q1	q0	q7....
OUT	1	7	5	3	1	7	5	4	3	2	1	0	7....

(ii) The Purpose :

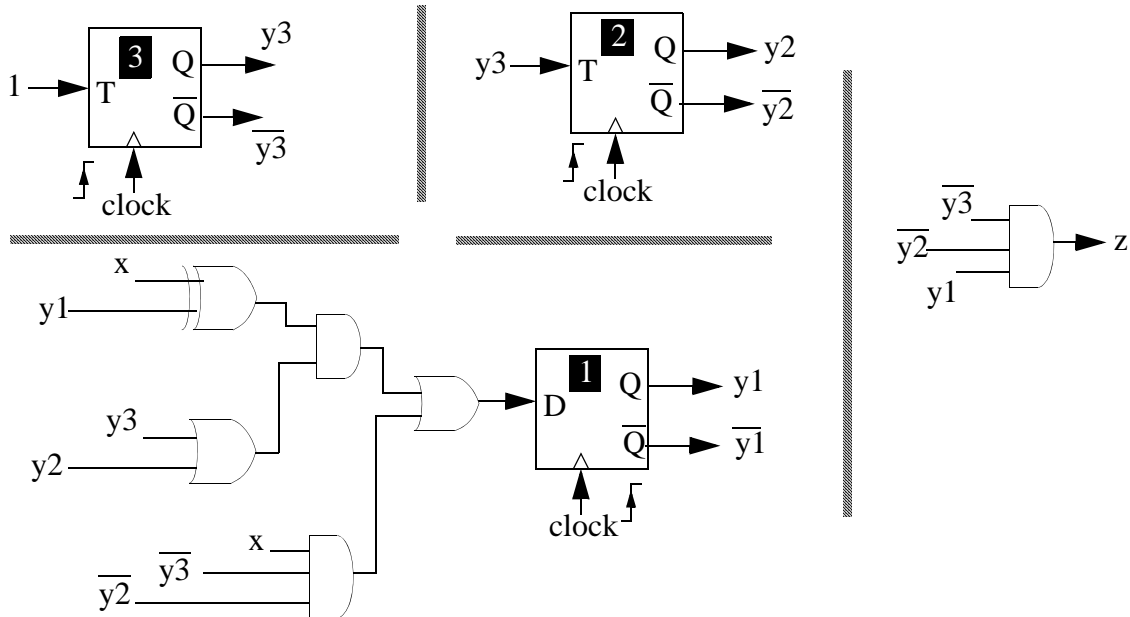
- It is a 3-bit counter that
- => counts down by 1 when input x is 0
- => counts down 2 when x is 1

This is a Moore circuit since the sequential circuit outputs do not depend on input x. This can also be seen from the sequential circuit output equations which do not contain x.

Q8) Consider the following sequential circuit with one input and one output :



Its internal circuit is shown below :



Analyze the sequential circuit as shown in class.

A8)

a) The FF input equations and the sequential circuit output equation :

$$\begin{aligned}
 T_3 &= 1 \\
 T_2 &= y_3 \\
 D_1 &= xy_3\bar{y}_2 + (y_3 + y_2)(x \oplus \bar{y}_1) \\
 &= xy_3\bar{y}_2 + (y_3 + y_2)(xy_1 + \bar{x}\bar{y}_1) \\
 &= xy_3\bar{y}_2 + xy_3y_1 + \bar{x}y_2y_1 + xy_3y_1 + xy_2y_1 \\
 z &= y_3\bar{y}_2y_1
 \end{aligned}$$

b) Next state equations :

$$\begin{aligned}
 \rightarrow y_3 &= T_3y_3 + \bar{T}_3\bar{y}_3 = 1y_3 + \bar{1}\bar{y}_3 = y_3 \\
 \rightarrow y_2 &= T_2y_2 + \bar{T}_2\bar{y}_2 = y_3y_2 + \bar{y}_3\bar{y}_2 \\
 \rightarrow y_1 &= D_1 \\
 &= xy_3\bar{y}_2 + xy_3y_1 + \bar{x}y_2y_1 + xy_3y_1 + xy_2y_1
 \end{aligned}$$

Note that output z is **not** a function of input x , thus, this is a **Moore** circuit. Also, this is a **non-finite memory** circuit since the state table below is not the standard state table for three FFs.

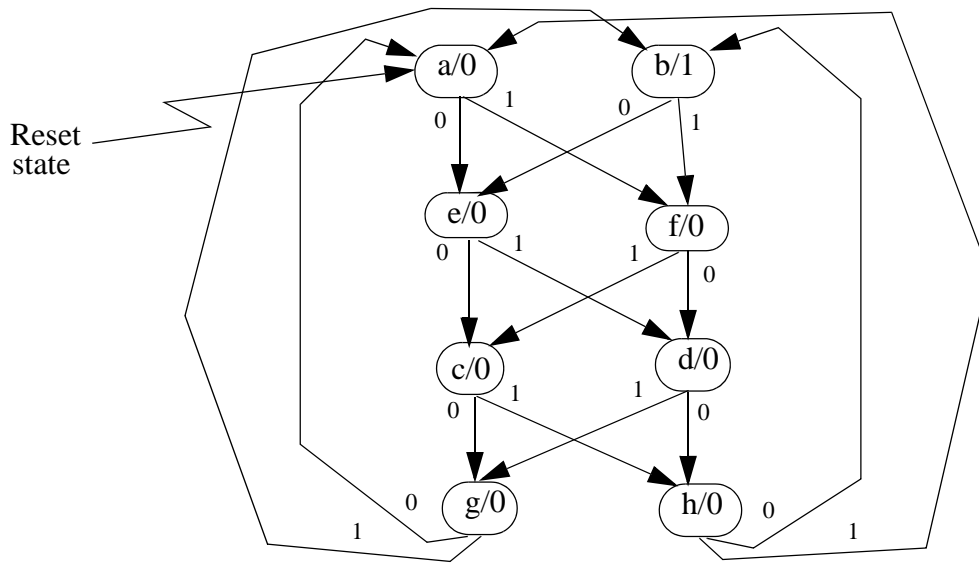
c) The excitation table :

y ₃ y ₂ y ₁	→ → →		z	
	y ₃ x=0	y ₂ y ₁ x=1	x=0	x=1
000	100	101	0	0
001	100	101	1	1
010	110	111	0	0
011	111	110	0	0
100	010	011	0	0
101	011	010	0	0
110	000	001	0	0
111	001	000	0	0

d) The state table :

PS	NS		OUT	
	x=0	x=1	x=0	x=1
a	e	f	0	0
b	e	f	1	1
c	g	h	0	0
d	h	g	0	0
e	c	d	0	0
f	d	c	0	0
g	a	b	0	0
h	b	a	0	0

e) The state diagram :



f) The purpose of the circuit : (i) The timing analysis : assume that the following input sequence is applied to the sequential circuit. Also assume that the initial state is “a.” Then :

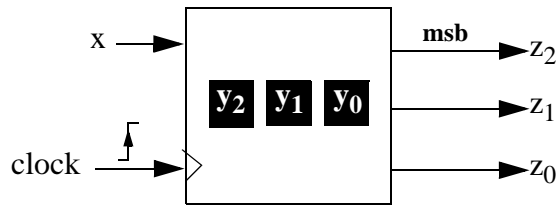
x 1 0 1 1 0 1 0 1 1 0 0 0 0 1 time

time	t0	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11	t12	t13
x	1	0	1	1	0	1	0	1	1	0	0	0	0	1
PS	a	f	d	g	b	e	d	h	a	f	d	h	b	e
OUT	0	0	0	0	1	0	0	0	0	0	0	0	1	0

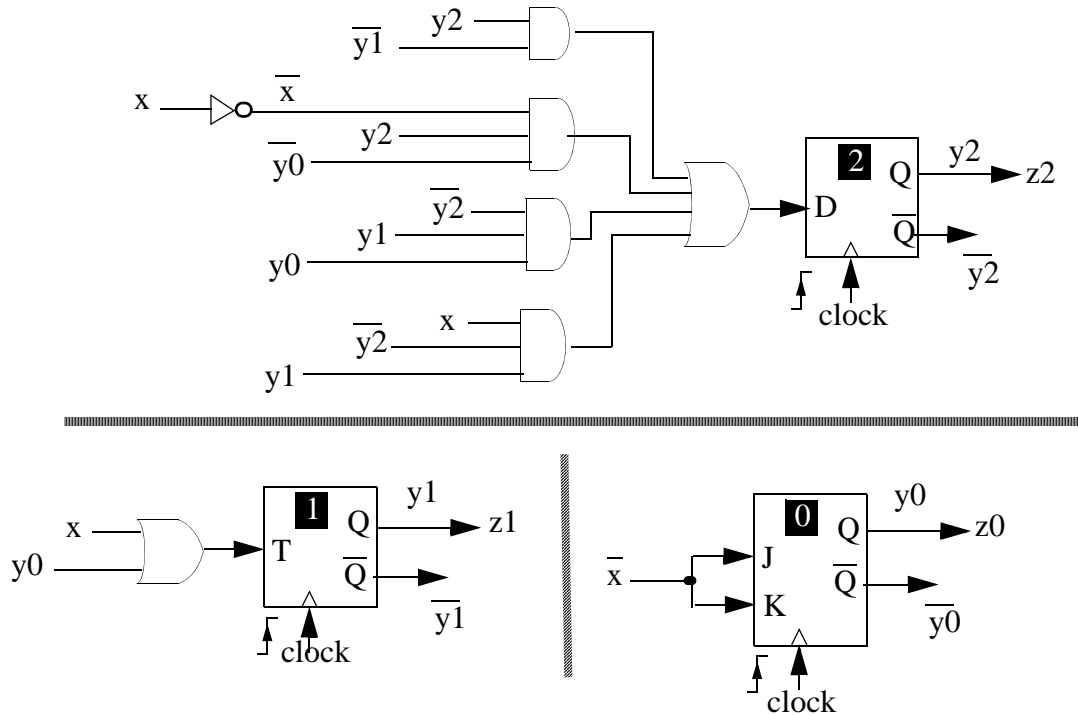
(ii) The purpose : the circuit outputs a 1 one clock period after odd number of 1s are received on a **nonoverlapping** four-bit input sequence. States a and b are the starting and ending states to check for a new sequence of four bits. If

a sequence ends with state “a” then the sequence did **not** have odd number of 1s. Otherwise, if the sequence ends with state “b” then it means the sequence had odd number of 1s. For example, above at t4 a new four-bit sequence starts with state b. The four-bit sequence is 0101 takes us to state a in t8 during which the output is 0. This is because, the sequence 0101 does **not** has odd number of 1s. The next four-bit sequence, starting at t8 is 1000, leading to state b in t12 and the output in t12 is 1 since the sequence 1000 has odd number of 1s.

Q9) Consider the following 1-input, 3-output **sequential** circuit with **three** flip-flops :



FF “y₂” is the most significant FF. The internal circuitry is shown below :



Continue the analysis of the sequential circuit to determine its purpose as shown **in class**.

Is this circuit a **Mealy** or **Moore** circuit ? Explain why.

A9) The analysis of the sequential circuit :

a) The FF input equations :

$$D2 = y_2\bar{y}_1 + \bar{x}y_2\bar{y}_0 + \bar{y}_2y_1y_0 + x\bar{y}_2y_1$$

$$T1 = x + y_0$$

$$J0 = K0 = \bar{x}$$

The sequential circuit output equations :

$$z_2 = y_2$$

$$z_1 = y_1$$

$$z_0 = y_0$$

b) Next state equations :

$$\begin{aligned} \overrightarrow{y_2} &= D2 = y_2\bar{y}_1 + \bar{x}y_2\bar{y}_0 + \bar{y}_2y_1y_0 + x\bar{y}_2y_1 \\ \overrightarrow{y_1} &= T1\bar{y}_1 + \bar{T}1y_1 = (x + y_0)\bar{y}_1 + \overline{(x + y_0)}y_1 \\ &= x\bar{y}_1 + \bar{y}_1y_0 + (\bar{x}\bar{y}_0)y_1 = x\bar{y}_1 + \bar{y}_1y_0 + \bar{x}\bar{y}_0y_1 \\ \overrightarrow{y_0} &= J0\bar{y}_0 + \bar{K}0y_0 = \bar{x}\bar{y}_0 + \bar{\bar{x}}y_0 = \bar{x}\bar{y}_0 + xy_0 \end{aligned}$$

This is a **Moore** circuit : The sequential circuit outputs are independent of x : $z_2 = y_2$ & $z_1 = y_1$ & $z_0 = y_0$.

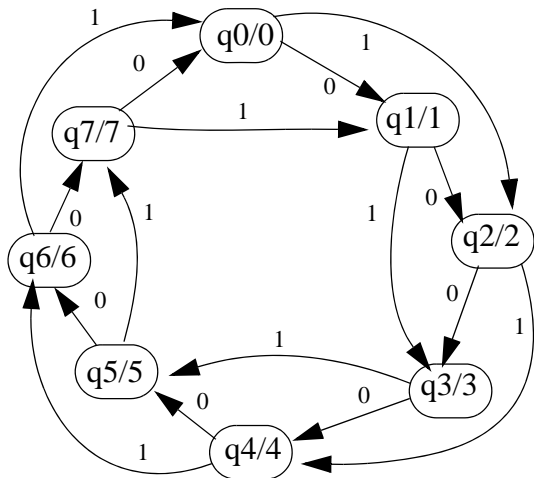
c) The excitation table :

	$y_2 y_1 y_0$	$\overrightarrow{y_2} \overrightarrow{y_1} \overrightarrow{y_0}$		$z_2 z_1 z_0$	
		$x=0$	$x=1$	$x=0$	$x=1$
q0	000	0 0 1	0 1 0	000	000
q1	001	0 1 0	0 1 1	001	001
q2	010	0 1 1	1 0 0	010	010
q3	011	1 0 0	1 0 1	011	011
q4	100	1 0 1	1 1 0	100	100
q5	101	1 1 0	1 1 1	101	101
q6	110	1 1 1	0 0 0	110	110
q7	111	0 0 0	0 0 1	111	111

d) The state table :

PS	NS		OUT
	$x=0$	$x=1$	
q0	q1	q2	0
q1	q2	q3	1
q2	q3	q4	2
q3	q4	q5	3
q4	q5	q6	4
q5	q6	q7	5
q6	q7	q0	6
q7	q0	q1	7

e) The state diagram :



f) The functional description :

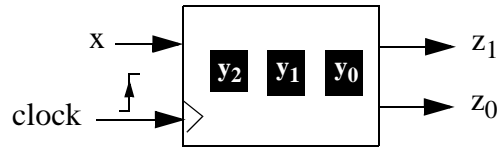
(i) Timing analysis :

Time	t0	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	...
x	1	1	1	1	0	0	0	0	0	1	1	...
PS	q7	q1	q3	q5	q7	q0	q1	q2	q3	q4	q6	...
OUT	7	1	3	5	7	0	1	2	3	4	6	...

(ii) The Purpose : This is a 3-bit Up counter that count up

- by 1 when x is 0 : 3, 4, 5, 6, 7, 0, 1, 2,...
- by 2 when x is 1 : 7, 1, 3, 5, 7, 1, 3, 5,...

Q10) Consider the following 1-input, 2-output sequential circuit with three flip-flops :



FF y_2 is the most significant FF. The first two analysis steps are already completed. The following are sequential circuit output equations and next flip-flop output (next state) equations :

$z_1 = y_1$ $z_0 = y_0$	$y_2 = \bar{x} y_2 + y_2 y_0 + y_2 y_1 + x y_1 y_0$	$y_1 = \bar{x} y_1 + y_1 y_0 + \bar{y}_2 y_1 + x \bar{y}_2 y_0$	$y_0 = x y_1 \bar{y}_0 + \bar{x} y_0 + x \bar{y}_2 y_1 + x \bar{y}_2 \bar{y}_0$
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Continue the analysis of the sequential circuit as shown in class. Is this circuit is a Mealy or Moore circuit ? Explain why ?

A10) The analysis steps continue with the excitation table and state table steps below :

c) The excitation table :

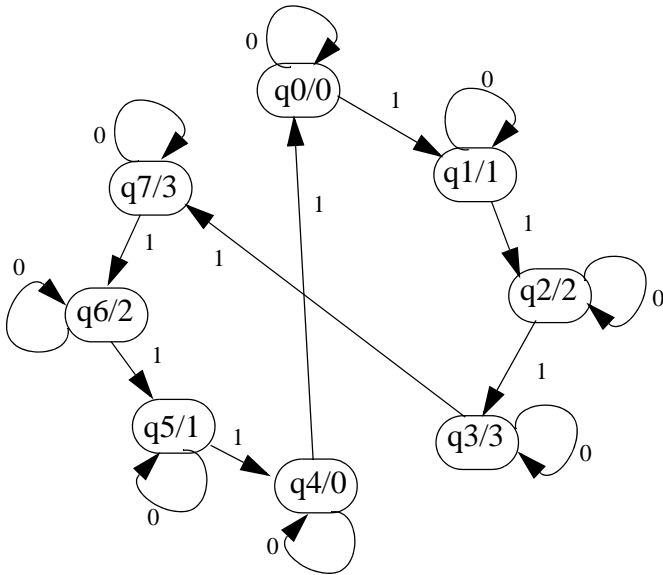
$y_2 y_1 y_0$	$y_2 y_1 y_0$		$z_1 z_0$	
	$x=0$	$x=1$	$x=0$	$x=1$
000	000	001	00	00
001	001	010	01	01
010	010	011	10	10
011	011	111	11	11
100	100	000	00	00
101	101	100	01	01
110	110	101	10	10
111	111	110	11	11

d) The state table :

PS	NS		OUT
	$x=0$	$x=1$	
q0	q0	q1	0
q1	q1	q2	1
q2	q2	q3	2
q3	q3	q7	3
q4	q4	q0	0
q5	q5	q4	1
q6	q6	q5	2
q7	q7	q6	3

This is a **Moore** circuit since the sequential circuit outputs do not depend on input x. This can also be seen from the sequential circuit output equations which do not contain x.

e) The state diagram :



f) The functional description :

We see that there are state changes if the input is 1. Therefore, we apply 1s to determine the purpose.

(i) Timing analysis :

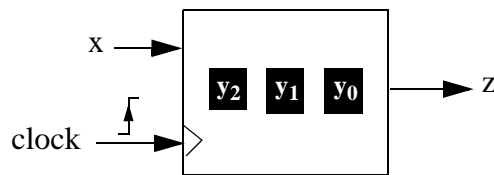
Time	t0	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10...
x	1	1	1	1	1	1	1	1	1	0	1....
PS	q1	q2	q3	q7	q6	q5	q4	q0	q1	q2....	
OUT	1	2	3	3	2	1	0	0	1	2	2....

(ii) The Purpose :

It is a modified **2-bit binary up and down counter**.that counts when input x is 1. It counts as 1, 2, 3, 3, 2, 1, 0, 0, 1, 2, 3, 3, 2,...

The count does **not** change when x is 0.

Q11) Consider the following **1-input, 1-output sequential** circuit :



The sequential circuit contains **three** flip-flops. FF y_2 is the most significant FF.

The first two analysis steps are already completed. The following are next flip-flop output equations and the sequential circuit **output** equation :

$$\overline{y_2} \rightarrow y_2 y_1 \overline{y_0} + x y_2 \overline{y_1} + y_2 \overline{y_1} y_0 + x \overline{y_2} y_1 y_0$$

$$\overline{y_1} \rightarrow y_2 y_1 \overline{y_0} + x y_1 \overline{y_0} + y_2 \overline{y_1} y_0 + x \overline{y_1} y_0$$

$$\overline{y_0} \rightarrow y_2 y_1 \overline{y_0} + x \overline{y_0}$$

$$z = y_2 \overline{y_1} y_0 + y_2 y_1 \overline{y_0}$$

Continue the analysis of the sequential circuit as shown **in class**.

After doing the timing analysis, if you **cannot** figure out the purpose, just write "I cannot determine the purpose."

Is this circuit a **Mealy** or **Moore** circuit ? Explain why.

Is this a **non-finite** memory or **finite** memory circuit ? Explain why.

A11) The following equations are given :

$$\vec{y}_2 = y_2 y_1 \bar{y}_0 + x y_2 \bar{y}_1 + \bar{y}_2 y_1 y_0 + \bar{x} \bar{y}_2 y_1 y_0$$

$$\vec{y}_1 = y_2 y_1 \bar{y}_0 + x y_1 \bar{y}_0 + y_2 \bar{y}_1 y_0 + \bar{x} \bar{y}_1 y_0$$

$$\vec{y}_0 = y_2 y_1 \bar{y}_0 + \bar{x} \bar{y}_0$$

$$z = y_2 \bar{y}_1 y_0 + y_2 y_1 \bar{y}_0$$

This is a **Moore** circuit : The sequential circuit output, z, is independent of x. That is, the z equation does not contain "x" as one of the variables. The analysis of the sequential circuit is continued :

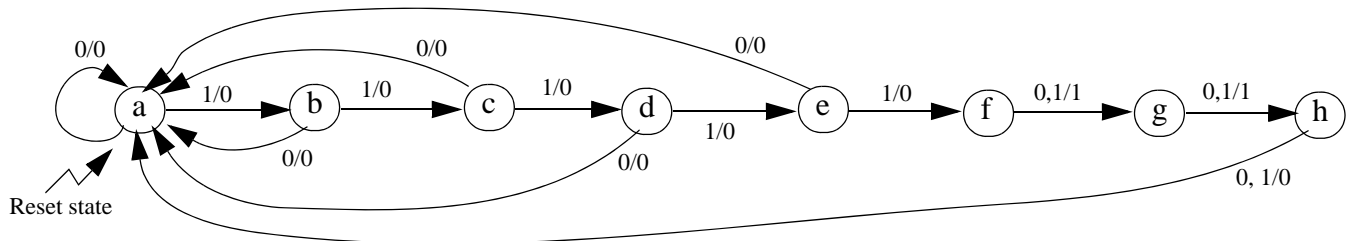
c) The excitation table :

	$y_2 y_1 y_0$	$\vec{y}_2 \vec{y}_1 \vec{y}_0$		z2 z1 z0	
		x=0	x=1	x=0	x=1
a	000	0 0 0	0 0 1	0	0
b	001	0 0 0	0 1 0	0	0
c	010	0 0 0	0 1 1	0	0
d	011	0 0 0	1 0 0	0	0
e	100	0 0 0	1 0 1	0	0
f	101	1 1 0	1 1 0	1	1
g	110	1 1 1	1 1 1	1	1
h	111	0 0 0	0 0 0	0	0

d) The state table :

PS	NS		OUT	
	x=0	x=1	x=0	x=1
a	a	b	0	0
b	a	c	0	0
c	a	d	0	0
d	a	e	0	0
e	a	f	0	0
f	g	g	1	1
g	h	h	1	1
h	a	a	0	0

e) The state diagram :



f) The functional description :

(i) Timing analysis :

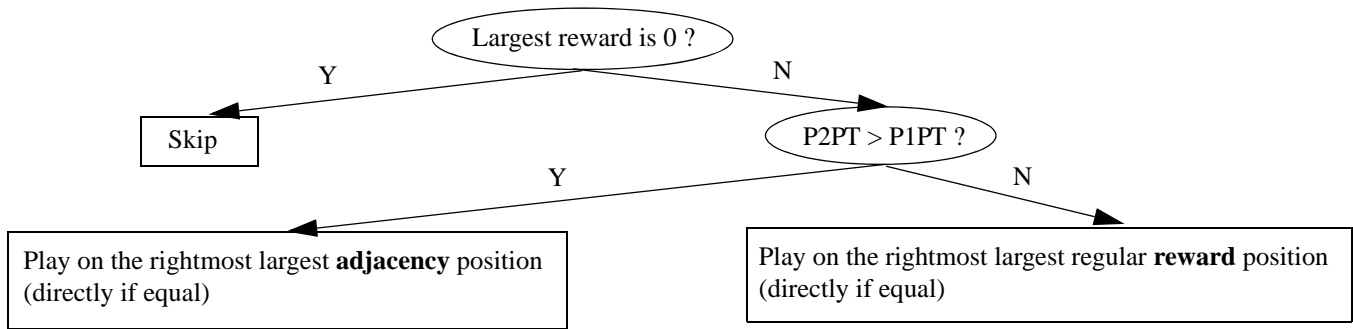
Time	t0	t1	t2	t3	t4	t5	t6	t7	t8	t9	t10	t11	t12	t13	t14	t15	t16	t17	t18	t19
x	0	1	1	1	1	1	0	1	1	0	0	1	1	1	1	1	0	0	1	1
PS	a	a	b	c	d	e	f	g	h	a	a	a	b	c	d	e	f	g	h	a
OUT	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0

(ii) Purpose : This is a sequence detector that checks for 5 (five) consecutive 1s : $x \xrightarrow{\text{Time}} 11111XXX$
 $z \quad 00000110$

Thus, it has a cycle of eight (8) clock periods. Then, it starts checking again. If it receives an incorrect bit, it starts a new sequence. There are **no** overlapped sequences.

This is a **non-finite memory** sequential circuit since it does **not** have standard state table for a finite input memory circuit with three flip-flops.

Q12) Consider the **Ppm** term project. Assume that the playing strategy of the **machine** player is as follows :



Consider the following table that shows the random digit, if the machine player is ahead **before** the play, position displays **before** and **after** the **machine** player plays, whether the random digit is played directly or added, the number of adjacencies, the points earned by the **machine** player and whether the machine player plays again :

RD	P2PT > P1PT	Displays Before Play				Displays After Play				D/A	The Adjacency	Points Earned (Decimal)	Machine player plays again
		PD3	PD2	PD1	PD0	PD3	PD2	PD1	PD0				
5	Y	A	4	9	4	A	4	9	9	A	1	18	Yes
1	Y	1	0	1	E								
2	N	E	C	C	E								
0	N	F	0	0	F								
8	Y	F	7	7	F								

Assume that the code is **EF**.

The first row shows how the random digit is played by the **machine** player. A circle is drawn on a position if it is played on. The meaning of **D/A** is Direct/Add which is whether the machine player plays the random digit **directly** on a position or by **adding** to a position.

Note that the cases are **independent** of each other. That is, they do **not** necessarily follow each other with respect to time.

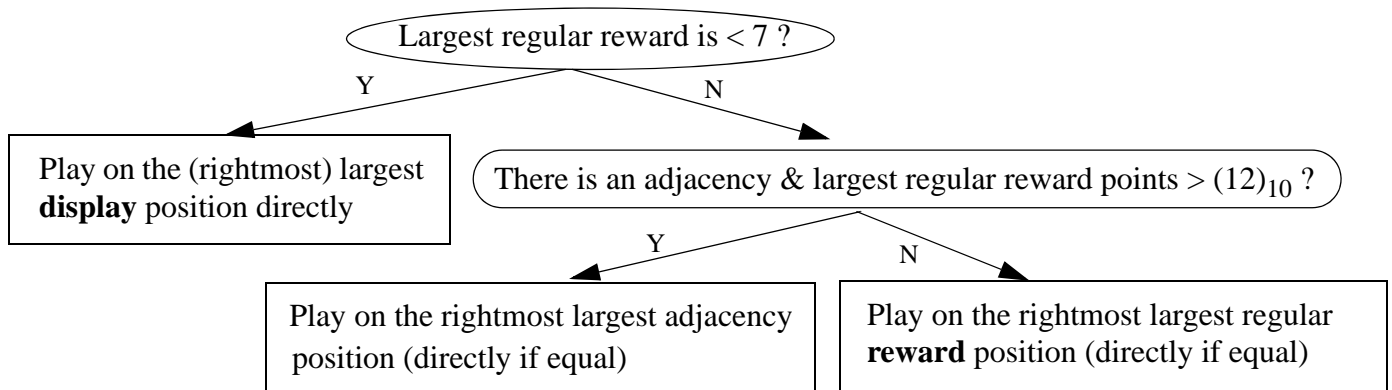
Complete the table.

A12) The table is completed below. Those entries to be filled out are shown in bold. The positions played on are shown by circles.

RD	P2PT > P1PT	Displays Before Play PD3 PD2 PD1 PD0	Displays After Play PD3 PD2 PD1 PD0	D/A	The Adjacency	Points Earned (Decimal)	Machine player plays again
5	Y	A 4 9 4	A 4 9 (9)	A	1	18	Yes
1	Y	1 0 1 E	1 (1) 1 E	D	2	4	Yes
2	N	E C C E	E C (E) E	A	1	140	Yes
0	N	F 0 0 F	F 0 0 (F)	A	0	135	No
8	Y	F 7 7 F	F 7 7 (7)	A	2	28	Yes

Note that the machine player does **not** check for code digits and so misses large reward points on rows 2 and 5. The random digits on these rows enable it to play the code digits.

Q13) Consider the **Ppm** term project. Assume that the playing strategy of the **machine** player is as follows :



Consider the following table that shows the random digit, position displays **before** and **after** the **machine** player plays, whether the random digit is played directly or added, the number of adjacencies, the points earned by the **machine** player and whether the machine player plays again :

RD	Displays Before Play PD3 PD2 PD1 PD0	Displays After Play PD3 PD2 PD1 PD0	D/A	The Adjacency	Points Earned (Decimal)	Machine player plays again
9	F 5 7 8					
2	E 2 F E					
3	4 7 1 C					
6	F F F F					
7	2 9 2 9					

Assume that the code is **9E**.

A circle is drawn on a position if it is played on. The meaning of **D/A** is Direct/Add which is whether the player plays the random digit **directly** on a position or by **adding** to a position.

Note that the cases are **independent** of each other. That is, they do not necessarily follow each other with respect to time.

Complete the table.

A13) The table is completed below. The displays played on are shown in bold and circled :

RD	Displays Before Play				Displays After Play				D/A	The Adjacency	Points Earned (Decimal)	Machine player plays again
	PD3	PD2	PD1	PD0	PD3	PD2	PD1	PD0				
9	F	5	7	8	F	(E)	7	8	A	0	14	N
2	E	2	F	E	E	2	(2)	E	D	1	4	Y
3	4	7	1	C	(7)	7	1	C	A	1	14	Y
6	F	F	F	F	F	F	F	(6)	D	0	6	N
7	2	9	2	9	2	9	(9)	9	A	2	108	Y

We observe that the machine player misses a chance to earn code reward points on the first row when RD is 9. But, by chance, it earns code reward points when RD is 7 on the last row.