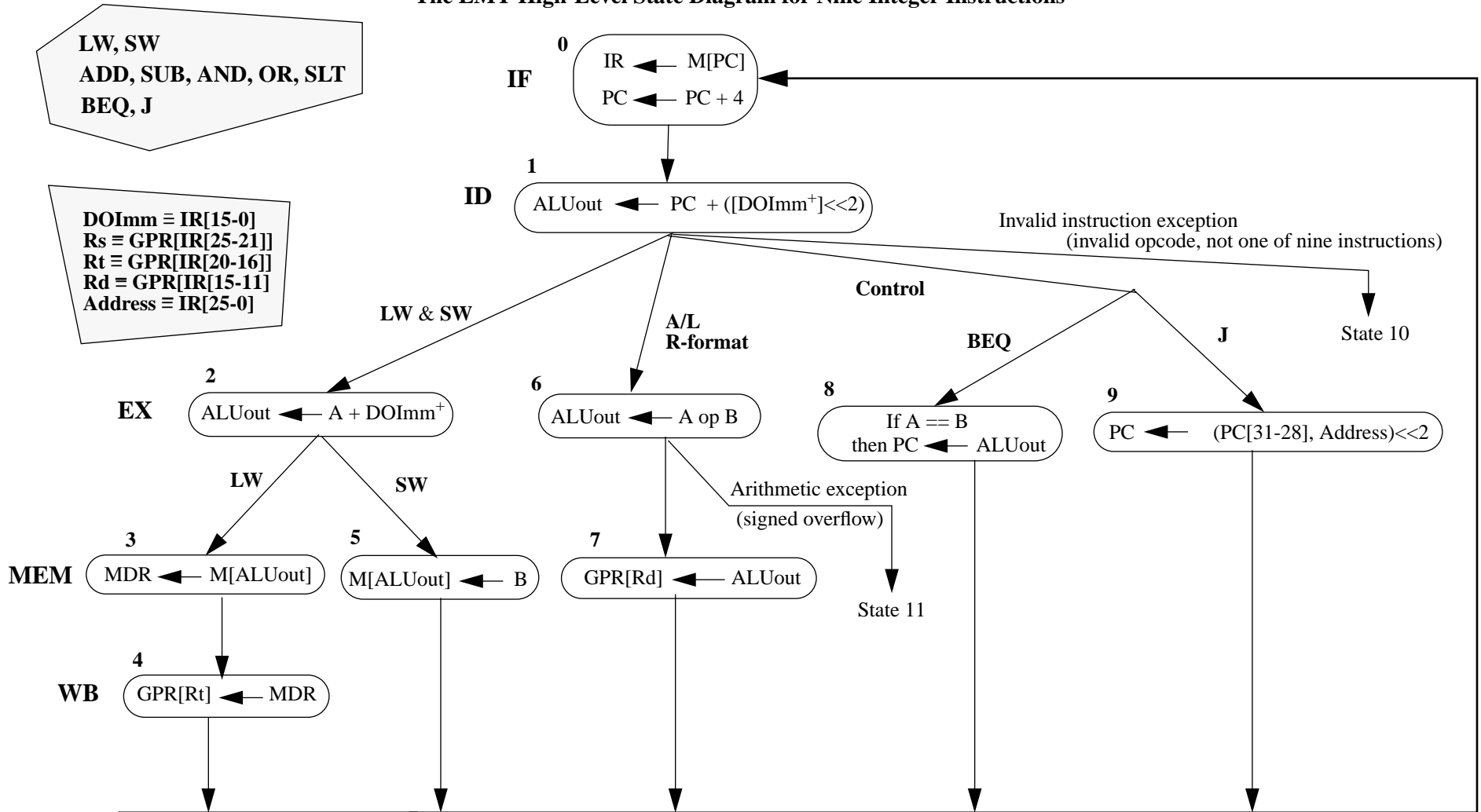
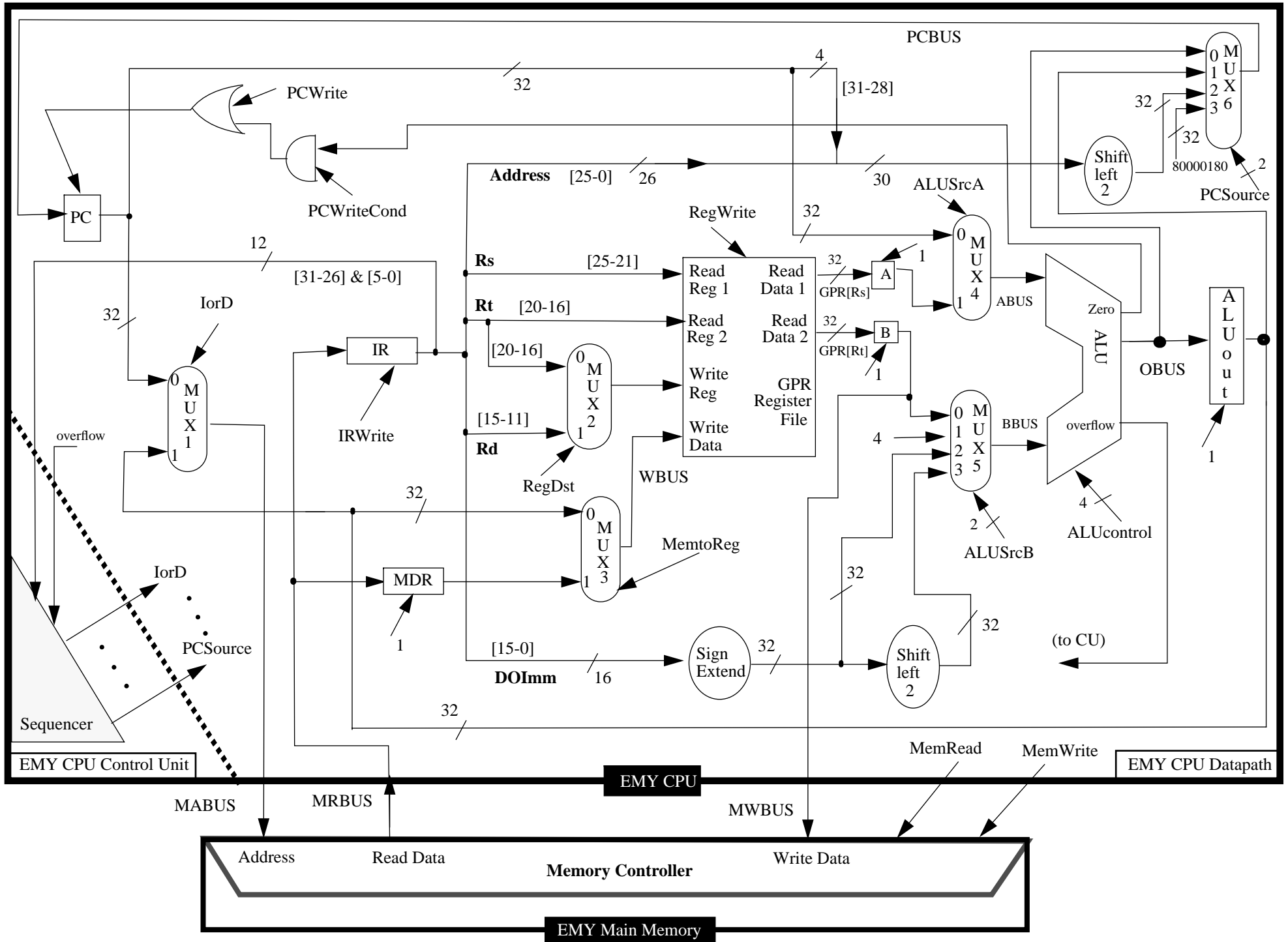


# EMY CPU

The EMY High-Level State Diagram for Nine Integer Instructions



- > A and B are **organizational** registers. Registers A and B get a value from GPR registers Rs and Rt **every** clock period :
  - $\Rightarrow$  A and B are stored (clocked) every clock period : A  $\leftarrow$  GPR[Rs] & B  $\leftarrow$  GPR[Rt] happens in **every** state (in every clock period for every instruction).
- > ALUout is also an **organizational** register and clocked **every** clock period. But, the input is **not** the same all the time as seen in states 1, 2 and 6.



### EMY Low-Level State Diagram for Nine (9) Integer Instructions

ALUOp	ALU operation	ALUcontrol
00	Add	0010
01	Sub	0110
10	indicated by function field of IR :	
	Add	0010
	Sub	0110
	And	0000
	Or	0001
	SLT	0111

