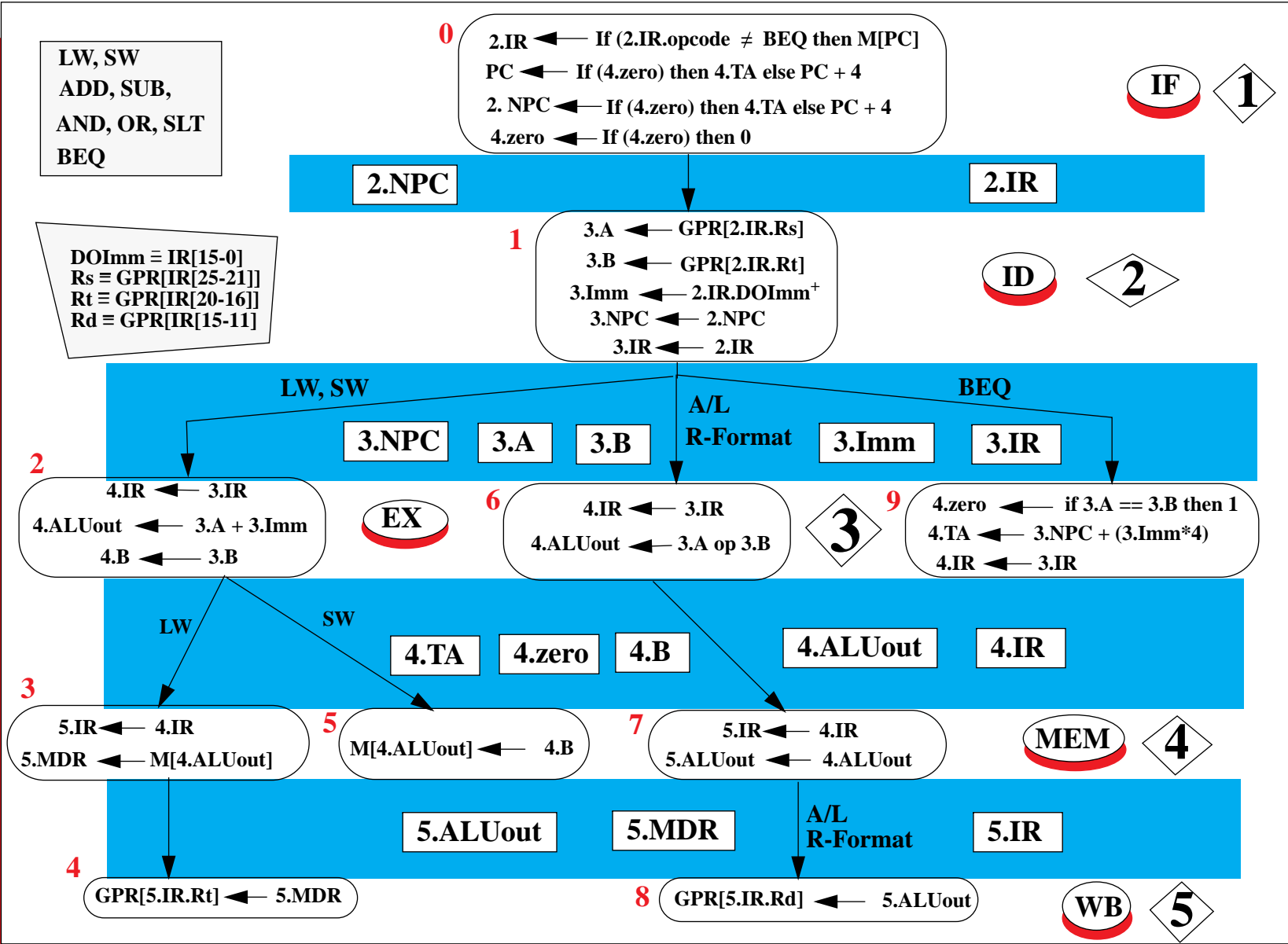
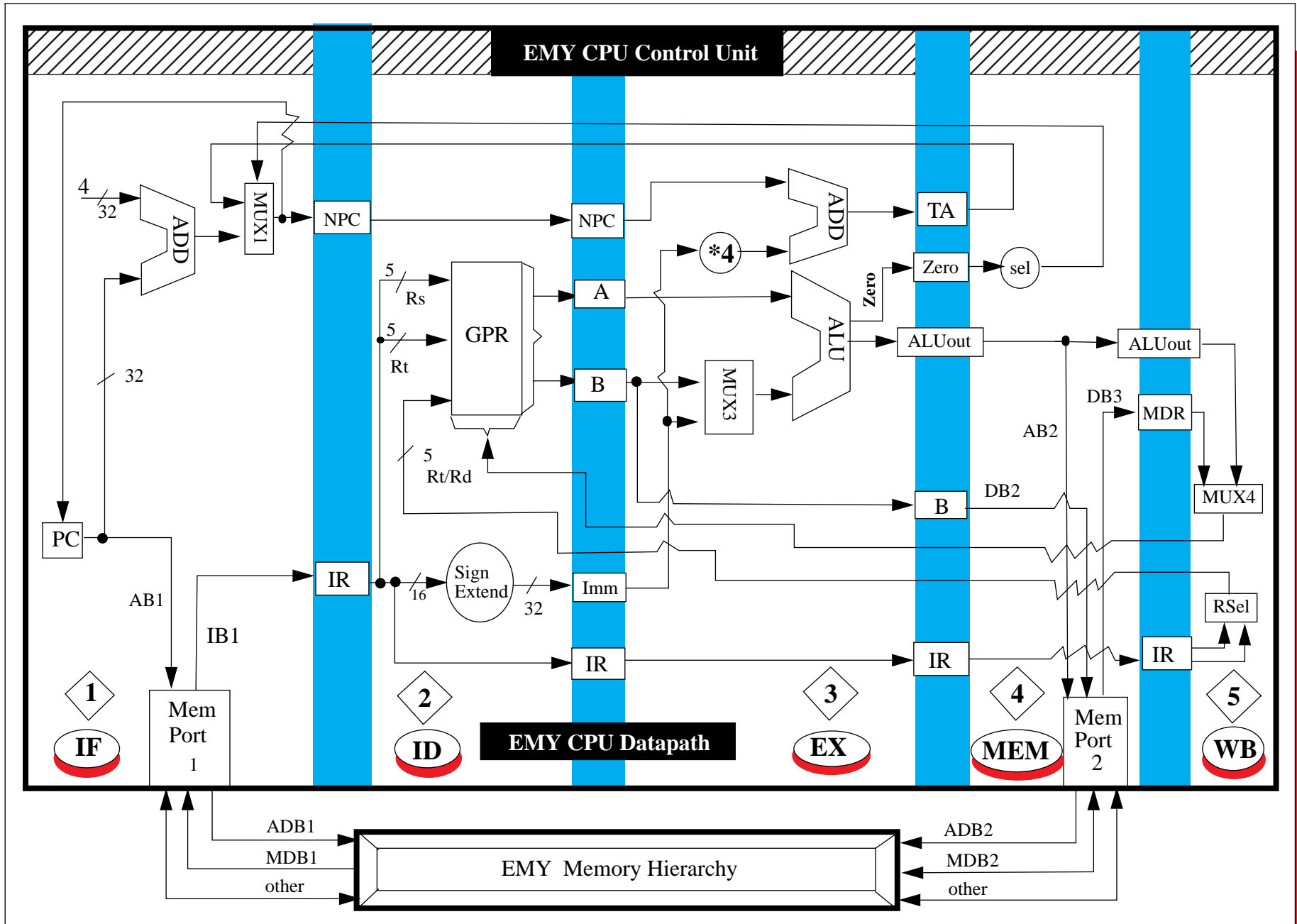


Pipelined EMP CPU without Forwarding and Delayed Branches



The Pipelined EMP CPU State Diagram for Eight MIPS Integer Instructions



The Pipelined EMY CPU Datapath for Eight MIPS *Integer* Instructions