

EXAM I ANSWERS

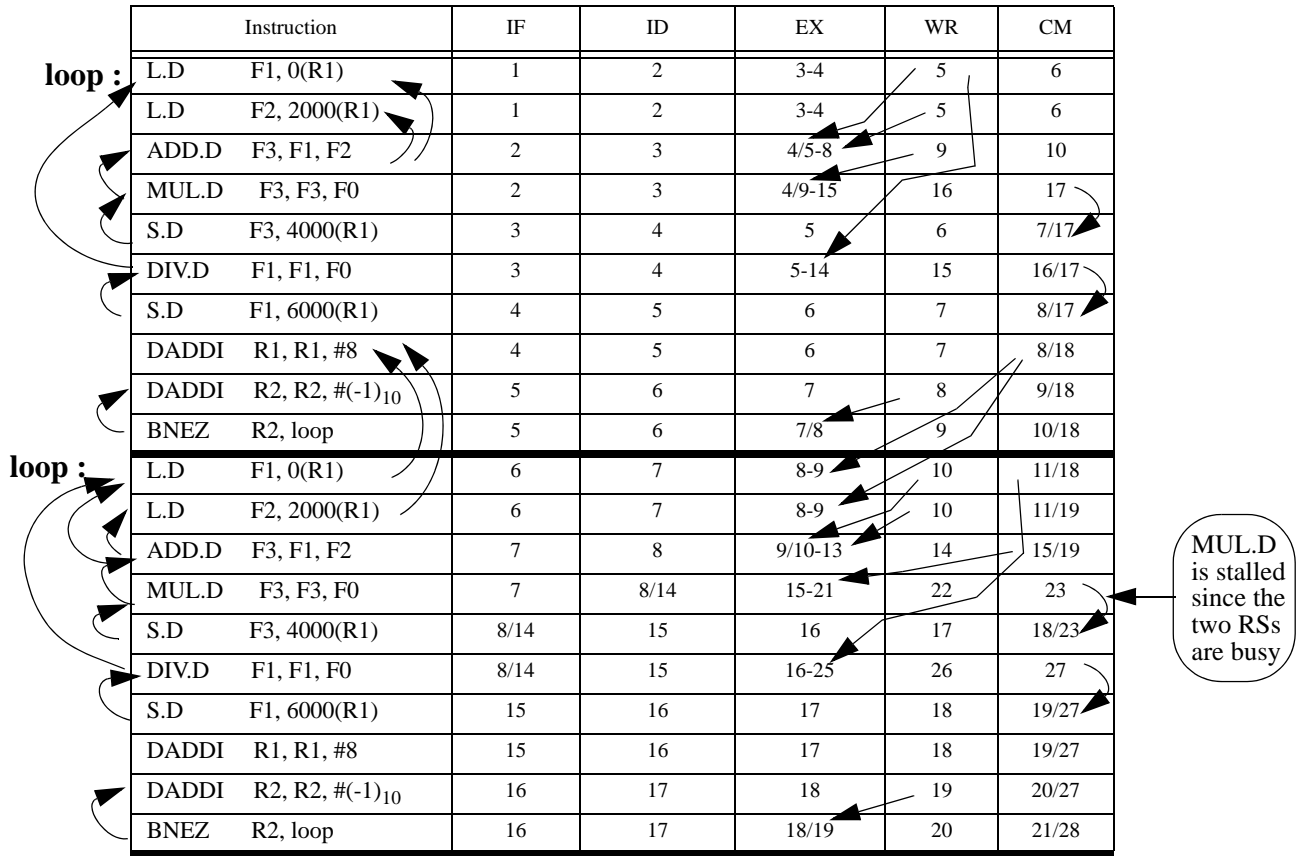
1) The execution of the loop with a reordered code and two iterations on the version 2 MIPS is as follows :

	Instruction	IF	ID	EX	MEM	WB
loop :	L.D F1, 0(R1)	1	2	3	4	5
	L.D F2, 2000(R1)	2	3	4	5	6
	DIV.D F1, F1, F0	3	4	5-14	15	16
	ADD.D F3, F1, F2	4	5	6-9	10	11
	DADDI R1, R1, #8	5	6	7	8	9
	MUL.D F3, F3, F0	6	7/9	10-16	17	18
	DADDI R2, R2, #(-1) ₁₀	7/9	10	11	12	13
	S.D F3, 3FF8(R1)	10	11/15	16	17	
	BNEZ R2, loop	11/15	16			
Branch delay slot	S.D F1, 5FF8(R1)	16	17	18	19	
loop :	L.D F1, 0(R1)	17	18	19	20	21
	L.D F2, 2000(R1)	18	19	20	21	22
	DIV.D F1, F1, F0	19	20	21-30	31	32
	ADD.D F3, F1, F2	20	21	22-25	26	27
	DADDI R1, R1, #8	21	22	23	24	25
	MUL.D F3, F3, F0	22	20/25	26-32	33	34
	DADDI R2, R2, #(-1) ₁₀	23/25	26	27	28	29
	S.D F3, 3FF8(R1)	26	27/31	32	33	
	BNEZ R4, loop	27/31	32			
Branch delay slot	S.D F1, 5FF8(R1)	32	33	34	35	

The code execution ends in clock period 35 !

All data hazards are RAW.

2) The execution of the loop with **two** iterations on the *version 5 MIPS* with non-ideal memory is below. The execution of the code ends at clock period 28.



The code execution ends in clock period 28 !

All data hazards are RAW.

Note that we cannot reorder the instructions since the pipeline is designed to handle the old code !

3) The VLIW MIPS code is below.

	Mem 1	Mem 2	FP 1	FP 2	Int/Br
loop :	L.D F1, 0(R1)	L.D F4, 8(R1)			
	L.D F5, (16) ₁₀ (R1)	L.D F6, (24) ₁₀ (R1)			
	L.D F7, (32) ₁₀ (R1)	L.D F8, (40) ₁₀ (R1)	DIV.D F16, F1, F0	DIV.D F17, F4, F0	
	L.D F9, (48) ₁₀ (R1)	L.D F2, 2000(R2)	DIV.D F18, F5, F0	DIV.D F19, F6, F0	
	L.D F10, 2008(R2)	L.D F11, 2010(R2)	DIV.D F20, F7, F0	DIV.D F21, F8, F0	
	L.D F12, 2018(R2)	L.D F13, 2020(R2)	DIV.D F22, F8, F0	ADD.D F1, F1, F2	
	L.D F14, 2028(R2)	L.D F15, 2030(R2)	ADD.D F4, F4, F1	ADD.D F5, F5, F11	
			ADD.D F6, F6, F12	ADD.D F7, F7, F13	
			ADD.D F8, F8, F14	ADD.D F9, F9, F15	
				MUL.D F1, F1, F0	
			MUL.D F4, F4, F0	MUL.D F5, F5, F0	
	S.D F16, 6000(R1)	S.D F17, 6008(R1)	MUL.D F6, F6, F0	MUL.D F7, F7, F0	
	S.D F18, 6010(R1)	S.D F19, 6018(R1)	MUL.D F8, F8, F0	MUL.D F9, F9, F0	
	S.D F20, 6020(R1)	S.D F21, 6028(R1)			
	S.D F22, 6030(R1)				
		S.D F1, 4000(R1)			
	S.D F4, 4008(R1)	S.D F5, 4010(R1)			DADDI R2, R2, #(-7) ₁₀
S.D F6, 4018(R1)	S.D F7, 4020(R1)			BNEZ R4, loop	
S.D F8, 4028(R1)	S.D F9, 4030(R1)			DADDI R1, R1, #(56) ₁₀	

The loop is unrolled **seven** (7) times. Unrolling seven times is enough since the ADD+MUL group is independent of the DIV group, providing extra independent instructions for the DIV group. The ADD and MUL instructions are unrolled enough to eliminate NOPs.

Unrolling eight times or more would eliminate some NOPs, but the program would be large as more L.D, S.D, ADD.D, MUL.D and DIV.D instructions would be needed. Also, using the 32 FP registers would be harder.

4) a) The vectorized VMIPS code is as follows :

```

LV      V1, R1      ; Load vector A to V1
LV      V2, R3      ; Load vector B to V2
ADDV.D  V3, V1, V2  ; Calculate A[i] + B[i]
DIVVS.D V1, V1, F0  ; Calculate A[i] / k
MULVS.D V3, V3, F0  ; Calculate k * (A[i] + B[i])
SV      R4, V3      ; Store k* (A[i] + B[i]) to vector C
SV      R5, V1      ; Store A[i] / k to vector D
    
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b) The execution timing is as follows :

