The MIPS Unpipelined CPU State Diagram for *Integer* instructions

Section A.3, pages A-26 - A-30 => **Unpipelined** Integer MIPS CPU
The MIPS Unpipelined CPU Datapath for Integer instructions

Section A.3, pages A-26 - A-30 => Unpipelined Integer MIPS CPU
The MIPS Pipelined CPU State Diagram for Integer instructions

Section A.3, pages A-30 - A-39 => Pipelined Integer MIPS CPU

Note: Branch instructions take two (2) clock periods and there are delayed branches
The MIPS Pipelined CPU Datapath for Integer instructions

Forwardings are not shown

Section A.3, pages A-30 - A-39 => Pipelined Integer MIPS CPU