**From:** Programmable Logic Data Manual, Signetics, 1987


---

**Signetics**

**PLS100/PLS101**

Field-Programmable Logic Array (16 × 48 × 8)

Signetics Programmable Logic

**Product Specification**

---

**Application Specific Products**

- Series 28

**DESCRIPTION**

The PLS100 (Tri-state) and PLS101 (Open Collector) are bipolar, fuse Programmable Logic Arrays (FPLAs). Each device utilizes the standard AND/OR/Invert architecture to directly implement custom sum of product logic equations.

Each device consists of 16 dedicated inputs and 8 dedicated outputs. Each output is capable of being actively controlled by any or all of the 48 product terms. The True, Complement, or Don't Care condition of each of the 16 inputs can be ANDed together to comprise one P-term. All 48 P-terms can be selectively ORed to each output.

The PLS100 and PLS101 are fully TTL compatible, and chip enable control for expansion of input variables and output inhibit. They feature either Open Collector or Tri-state outputs for ease of expansion of product terms and application in bus-organized systems.

Order codes are contained on the pages following.

**FEATURES**

- Field-Programmable (NI-Cr link)
- Input variables: 16
- Output functions: 8
- Product terms: 48
- I/O propagation delay: 50ns (max.)
- Power dissipation: 600mW (typ.)
- Input loading: -100μA (max.)
- Chip Enable Input
- Output option:
  - PLS100: Tri-state
  - PLS101: Open-Collector
- Output disable function:
  - Tri-state: HI-Z
  - Open-Collector: High

**APPLICATIONS**

- CRT display systems
- Code conversion
- Peripheral controllers
- Function generators
- Look-up and decision tables
- Microprogramming
- Address mapping
- Character generators
- Data security encoders
- Fault detectors
- Frequency synthesizers
- 16-bit by 8-bit bus interface
- Random logic replacement

---

**PIN CONFIGURATIONS**

**N Package**

<table>
<thead>
<tr>
<th>PIN</th>
<th>Vcc</th>
<th>Vcc</th>
<th>Vcc</th>
<th>Vcc</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
<td>8</td>
<td>9</td>
<td>10</td>
<td>11</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
<td>3</td>
<td>4</td>
<td>5</td>
</tr>
<tr>
<td>12</td>
<td>13</td>
<td>14</td>
<td>15</td>
<td>16</td>
</tr>
</tbody>
</table>

**A Package**

**LOGIC FUNCTION**

**Typical Product Term:**

\[ P_n = A \cdot B \cdot C \cdot D \cdot \ldots \]

**Typical Logic Function:**

At Output Polarity = H

\[ Z = P_0 + P_1 + P_2 + \ldots \]

At Output Polarity = L

\[ Z = P_0 \cdot P_1 \cdot P_2 + \ldots \]

**NOTES:**

1. For each of the 8 outputs, either function Z (Active-High) or Z (Active-Low) is available, but not both.

2. The desired output polarity is programmed via the EX-OR gates.

3. Z, A, B, C, etc., are user defined connections to fixed inputs (0) and output pins (0).

---

November 19, 1986

6-3

853-0308 86602

C52204 Handout No: 14
Programmable logic arrays
(16 × 48 × 8)

LOGIC DIAGRAM

NOTES:
1. All AND gate inputs with a blown link float to a logic "1".
2. All OR gate inputs with a blown fuse float to logic "0".
3. Programmable connection.
Programmable logic arrays
(16 × 48 × 8)

FUNCTIONAL DIAGRAM

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>DESCRIPTION</th>
<th>3-STATE</th>
<th>OPEN COLLECTOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>28-Pin Plastic Dual In-Line 600mil-wide</td>
<td>PLS100N</td>
<td>PLS101N</td>
</tr>
<tr>
<td>28-Pin Plastic Leaded Chip Carrier</td>
<td>PLS100A</td>
<td>PLS101A</td>
</tr>
</tbody>
</table>

ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>RATINGS</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>VCC</td>
<td>Supply voltage</td>
<td>+7.0</td>
<td>Vdc</td>
</tr>
<tr>
<td>VIN</td>
<td>Input voltage</td>
<td>+5.5</td>
<td>Vdc</td>
</tr>
<tr>
<td>VDD</td>
<td>Output voltage</td>
<td>+5.5</td>
<td>Vdc</td>
</tr>
<tr>
<td>IIN</td>
<td>Input current</td>
<td>±30</td>
<td>mA</td>
</tr>
<tr>
<td>IOUT</td>
<td>Output current</td>
<td>+100</td>
<td>mA</td>
</tr>
<tr>
<td>TAMB</td>
<td>Operating temperature range</td>
<td>0 to +75</td>
<td>°C</td>
</tr>
<tr>
<td>TSTG</td>
<td>Storage temperature range</td>
<td>-65 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

NOTE:
1. Stresses above those listed may cause malfunction or permanent damage to the device. This is a stress rating only. Functional operation at these or any other conditions above those indicated in the operational and programming specification of the device is not implied.

THERMAL RATINGS

<table>
<thead>
<tr>
<th>TEMPERATURE</th>
<th>TEMP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Maximum junction</td>
<td>150°C</td>
</tr>
<tr>
<td>Maximum ambient</td>
<td>75°C</td>
</tr>
<tr>
<td>Allowable thermal rise ambient to junction</td>
<td>75°C</td>
</tr>
</tbody>
</table>

The PLS100 device is also processed to military requirements for operation over the military temperature range. For specifications and ordering information consult the Philips Components—Signetics Military Data Handbook.
LOGIC PROGRAMMING

PLS100/PLS101 is fully supported by industry standard (JEDEC compatible) PLD CAD tools, including Signetics' AMAZE, Data I/O Corporation's ABEL and Logical Devices Inc.'s CUPL design software packages.

All packages allow Boolean and state equation entry formats. ABEL and CUPL also accept, as input, schematic capture format. PLS100/PLS101 logic designs can also be generated using the program table entry format detailed on the following pages. This program table entry format is supported by the Signetics' AMAZE PLD design software (PTP module). AMAZE is available free of charge to qualified users.

To implement the desired logic functions, the state of each logic variable from logic equations (I, B, O, P, etc.) is assigned a symbol. The symbols for TRUE, COMPLEMENT, INACTIVE, PRESET, etc., are defined below.

OUTPUT POLARITY – (F)

```
<table>
<thead>
<tr>
<th>ACTIVE LEVEL</th>
<th>CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LOW (INVERTING)</td>
<td>L</td>
</tr>
<tr>
<td>HIGH (NON-INVERTING)</td>
<td>H</td>
</tr>
</tbody>
</table>
```

“AND” ARRAY – (I)

```
<table>
<thead>
<tr>
<th>STATE</th>
<th>CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>INACTIVE</td>
<td>0</td>
</tr>
<tr>
<td>I</td>
<td>H</td>
</tr>
<tr>
<td>I</td>
<td>L</td>
</tr>
<tr>
<td>DON'T CARE</td>
<td>-</td>
</tr>
</tbody>
</table>
```

“OR” ARRAY – (F)

```
<table>
<thead>
<tr>
<th>Pn STATUS</th>
<th>CODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACTIVE</td>
<td>A</td>
</tr>
<tr>
<td>INACTIVE</td>
<td>-</td>
</tr>
</tbody>
</table>
```

NOTES:
1. This is the initial unprogrammed state of all links. It is normally associated with all unused (inactive) AND gates Pn.
2. Any gate Pn will be unconditionally inhibited if any one of its (I) link pairs is left intact.

VIRGIN STATE

The PLS100/101 virgin devices are factory shipped in an unprogrammed state, with all fuses intact, such that:

1. All Pn terms are disabled (inactive) in the AND array.
2. All Pn terms are active in the OR array.
3. All outputs are Active-High.