TERM PROJECT DESIGN CHECKS

Syntactic Issues (-1 each)

1. a) Team information missing
   b) A name is missing
   c) Course name, section name, semester is missing

2. a) More than one schematic sheet used for design
   b) The circuit is spread all across the sheet
   c) Components are too close to each other
   d) Blocks (subcircuits) too close to each other
   e) Components of block too far from each other
   f) Wires with unnecessary turns
   g) Tangled/dangled wires
   h) Wires over components/labels/names
   i) Very long wires
   j) Labels/attributes/components overlap
   k) Components/wires not labelled

3. a) Unconnected components
   b) Input lines short circuited
   c) Output lines short circuited
   d) Component outputs short circuited to GND/VCC
   e) Component outputs unused

4. a) Experiment folder name is not correct
   b) Additional schematics and/or folders

Design Issues

5. a) The number of gates used too high
   b) The number of XDBs (Xilinx macros) used too high
   c) Incorrect programmable component usage
   d) Unnecessary buffers
   e) Unnecessary pads
   f) Unnecessary gates
   g) Unnecessary FFs
   h) Unnecessary XDBs
   i) Circuits are not in their appropriate places
   j) Previous experiments are not performed
   k) Last Xilinx process(es) not done

6. a) The circuit does not work completely (-30):

7. a) Other:

Draw the graph of the playing strategy on the other side

Other points assignments are shown on page 2
The Machine Player Strategy

Draw the graph of the strategy of your machine player below